

SECTION G — PHYSICS

G11 INFORMATION STORAGE

G11C STATIC STORES (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L 27/108-H01L 27/115; pulse technique in general H03K, e.g. electronic switches H03K 17/00)

Note(s) [2006.01]

1. This subclass covers devices or arrangements for storage of digital or analogue information:
 - i. in which no relative movement takes place between an information storage element and a transducer;
 - ii. which incorporate a selecting-device for writing-in or reading-out the information into or from the store.
2. This subclass does not cover elements not adapted for storage and not provided with such means as referred to in Note (3) below, which elements are classified in the appropriate subclass, e.g. of H01, H03K.
3. In this subclass, the following terms are used with the meaning indicated:
 - "storage element" is an element which can hold at least one item of information and is provided with means for writing-in or reading-out this information;
 - "memory" is a device, including storage elements, which can hold information to be extracted when desired.

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5/00 Details of stores covered by group G11C 11/00 [1, 2006.01]

- 5/02 • Disposition of storage elements, e.g. in the form of a matrix array [1, 2006.01]
- 5/04 • • Supports for storage elements; Mounting or fixing of storage elements on such supports [1, 2006.01]
- 5/05 • • • Supporting of cores in matrix [2, 2006.01]
- 5/06 • Arrangements for interconnecting storage elements electrically, e.g. by wiring [1, 2006.01]
- 5/08 • • for interconnecting magnetic elements, e.g. toroidal cores [1, 2006.01]
- 5/10 • • for interconnecting capacitors [1, 2006.01]
- 5/12 • Apparatus or processes for interconnecting storage elements, e.g. for threading magnetic cores [1, 2006.01]
- 5/14 • Power supply arrangements (auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413, G11C 11/4193; in general G05F, H02J, H02M) [5, 7, 2006.01]

7/00 Arrangements for writing information into, or reading information out from, a digital store

- (G11C 5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413, G11C 11/4193) [1, 2, 5, 2006.01]
- 7/02 • with means for avoiding parasitic signals [1, 2006.01]
 - 7/04 • with means for avoiding disturbances due to temperature effects [1, 2006.01]
 - 7/06 • Sense amplifiers; Associated circuits (amplifiers per se H03F, H03K) [1, 7, 2006.01]
 - 7/08 • • Control thereof [7, 2006.01]
 - 7/10 • Input/output [I/O] data interface arrangements, e.g. I/O data control circuits, I/O data buffers (level conversion circuits in general H03K 19/0175) [7, 2006.01]
 - 7/12 • Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines [7, 2006.01]
 - 7/14 • Dummy cell management; Sense reference voltage generators [7, 2006.01]

- 7/16 • Storage of analogue signals in digital stores using an arrangement comprising analogue/digital [A/D] converters, digital memories and digital/analogue [D/A] converters [7, 2006.01]
- 7/18 • Bit line organisation; Bit line lay-out [7, 2006.01]
- 7/20 • Memory cell initialisation circuits, e.g. when powering up or down, memory clear, latent image memory [7, 2006.01]
- 7/22 • Read-write [R-W] timing or clocking circuits; Read-write [R-W] control signal generators or management [7, 2006.01]
- 7/24 • Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells [7, 2006.01]
- 8/00 Arrangements for selecting an address in a digital store** (auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413, G11C 11/4193) [2, 5, 2006.01]
 - 8/02 • using selecting matrix [2, 2006.01]
 - 8/04 • using a sequential addressing device, e.g. shift register, counter (using first in first out [FIFO] registers for changing speed of digital data flow G06F 5/06; using last in first out [LIFO] registers for processing digital data by operating upon their order G06F 7/00) [5, 2006.01]
 - 8/06 • Address interface arrangements, e.g. address buffers (level conversion circuits in general H03K 19/0175) [7, 2006.01]
 - 8/08 • Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines [7, 2006.01]
 - 8/10 • Decoders [7, 2006.01]
 - 8/12 • Group selection circuits, e.g. for memory block selection, chip selection, array selection [7, 2006.01]
 - 8/14 • Word line organisation; Word line lay-out [7, 2006.01]
 - 8/16 • Multiple access memory array, e.g. addressing one storage element via at least two independent addressing line groups [7, 2006.01]
 - 8/18 • Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe [RAS] or column address strobe [CAS] signals [7, 2006.01]
 - 8/20 • Address safety or protection circuits, i.e. arrangements for preventing unauthorized or accidental access [7, 2006.01]
- 11/00 Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor** (G11C 14/00-G11C 21/00 take precedence) [1, 5, 2006.01]

Note(s) [2]

Group G11C 11/56 takes precedence over groups G11C 11/02-G11C 11/54.

 - 11/02 • using magnetic elements [1, 2006.01]
 - 11/04 • • using storage elements having cylindrical form, e.g. rod, wire (G11C 11/12, G11C 11/14 take precedence) [1, 2, 2006.01]
 - 11/06 • • using single-aperture storage elements, e.g. ring core; using multi-aperture plates in which each individual aperture forms a storage element [1, 2006.01]
 - 11/061 • • • using elements with single aperture or magnetic loop for storage, one element per bit, and for destructive read-out [2, 2006.01]
 - 11/063 • • • bit-organized, such as, 2L/2D-, 3D-organization, i.e. for selection of an element by means of at least two coincident partial currents both for reading and for writing [2, 2006.01]
 - 11/065 • • • word-organized, such as 2D-organization, or linear selection, i.e. for selection of all the elements of a word by means of a single full current for reading [2, 2006.01]
 - 11/067 • • • using elements with single aperture or magnetic loop for storage, one element per bit, and for non-destructive read-out [2, 2006.01]
 - 11/08 • • using multi-aperture storage elements, e.g. using transfluxors; using plates incorporating several individual multi-aperture storage elements (G11C 11/10 takes precedence; using multi-aperture plates in which each individual aperture forms a storage element G11C 11/06) [1, 2, 2006.01]
 - 11/10 • • using multi-axial storage elements [1, 2006.01]
 - 11/12 • • using tensors; using twistors, i.e. elements in which one axis of magnetisation is twisted [1, 2006.01]
 - 11/14 • • using thin-film elements [1, 2006.01]
 - 11/15 • • • using multiple magnetic layers (G11C 11/155 takes precedence) [2, 2006.01]
 - 11/155 • • • with cylindrical configuration [2, 2006.01]
 - 11/16 • • using elements in which the storage effect is based on magnetic spin effect [1, 2006.01]
 - 11/18 • using Hall-effect devices [1, 2006.01]
 - 11/19 • using non-linear reactive devices in resonant circuits [2, 2006.01]
 - 11/20 • • using parametrons [1, 2, 2006.01]
 - 11/21 • using electric elements [2, 2006.01]
 - 11/22 • • using ferroelectric elements [1, 2, 2006.01]
 - 11/23 • • using electrostatic storage on a common layer, e.g. Forrester-Haeff tubes (G11C 11/22 takes precedence) [2, 2006.01]
 - 11/24 • • using capacitors (G11C 11/22 takes precedence; using a combination of semiconductor devices and capacitors G11C 11/34, e.g. G11C 11/40) [1, 2, 5, 2006.01]
 - 11/26 • • using discharge tubes [1, 2, 2006.01]
 - 11/28 • • • using gas-filled tubes [1, 2, 2006.01]
 - 11/30 • • • using vacuum tubes (G11C 11/23 takes precedence) [1, 2, 2006.01]
 - 11/34 • • using semiconductor devices [1, 2, 2006.01]
 - 11/35 • • • with charge storage in a depletion layer, e.g. charge coupled devices [7, 2006.01]
 - 11/36 • • • using diodes, e.g. as threshold elements [1, 2, 2006.01]
 - 11/38 • • • • using tunnel diodes [1, 2, 2006.01]
 - 11/39 • • • using thyristors [5, 2006.01]
 - 11/40 • • • using transistors [1, 2, 2006.01]
 - 11/401 • • • • forming cells needing refreshing or charge regeneration, i.e. dynamic cells [5, 2006.01]
 - 11/402 • • • • with charge regeneration individual to each memory cell, i.e. internal refresh [5, 2006.01]
 - 11/403 • • • • with charge regeneration common to a multiplicity of memory cells, i.e. external refresh [5, 2006.01]
 - 11/404 • • • • • with one charge-transfer gate, e.g. MOS transistor, per cell [5, 2006.01]
 - 11/405 • • • • • with three charge-transfer gates, e.g. MOS transistors, per cell [5, 2006.01]

- 11/406 • • • • • Management or control of the refreshing or charge-regeneration cycles [5, 2006.01]
- 11/4063 • • • • • Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing or timing [7, 2006.01]
- 11/4067 • • • • • for memory cells of the bipolar type [7, 2006.01]
- 11/407 • • • • • for memory cells of the field-effect type [5, 2006.01]
- 11/4072 • • • • • Circuits for initialization, powering up or down, clearing memory or presetting [7, 2006.01]
- 11/4074 • • • • • Power supply or voltage generation circuits, e.g. bias voltage generators, substrate voltage generators, back-up power, power control circuits [7, 2006.01]
- 11/4076 • • • • • Timing circuits (for regeneration management G11C 11/406) [7, 2006.01]
- 11/4078 • • • • • Safety or protection circuits, e.g. for preventing inadvertent or unauthorised reading or writing; Status cells; Test cells (protection of memory contents during checking or testing G11C 29/52) [7, 2006.01]
- 11/408 • • • • • Address circuits [5, 2006.01]
- 11/409 • • • • • Read-write [R-W] circuits [5, 2006.01]
- 11/4091 • • • • • Sense or sense/refresh amplifiers, or associated sense circuitry, e.g. for coupled bit-line precharging, equalising or isolating [7, 2006.01]
- 11/4093 • • • • • Input/output [I/O] data interface arrangements, e.g. data buffers (level conversion circuits in general H03K 19/0175) [7, 2006.01]
- 11/4094 • • • • • Bit-line management or control circuits [7, 2006.01]
- 11/4096 • • • • • Input/output [I/O] data management or control circuits, e.g. reading or writing circuits, I/O drivers or bit-line switches [7, 2006.01]
- 11/4097 • • • • • Bit-line organisation, e.g. bit-line layout, folded bit lines [7, 2006.01]
- 11/4099 • • • • • Dummy cell treatment; Reference voltage generators [7, 2006.01]
- 11/41 • • • • forming cells with positive feedback, i.e. cells not needing refreshing or charge regeneration, e.g. bistable multivibrator or Schmitt trigger [5, 2006.01]
- 11/411 • • • • • using bipolar transistors only [5, 2006.01]
- 11/412 • • • • • using field-effect transistors only [5, 2006.01]
- 11/413 • • • • • Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing or power reduction [5, 2006.01]
- 11/414 • • • • • for memory cells of the bipolar type [5, 2006.01]
- 11/415 • • • • • Address circuits [5, 2006.01]
- 11/416 • • • • • Read-write [R-W] circuits [5, 2006.01]
- 11/417 • • • • • for memory cells of the field-effect type [5, 2006.01]
- 11/418 • • • • • Address circuits [5, 2006.01]
- 11/419 • • • • • Read-write [R-W] circuits [5, 2006.01]
- 11/4193 • • • • Auxiliary circuits specific to particular types of semiconductor storage devices, e.g. for addressing, driving, sensing, timing, power supply, signal propagation (G11C 11/4063, G11C 11/413 take precedence) [7, 2006.01]
- 11/4195 • • • • Address circuits [7, 2006.01]
- 11/4197 • • • • Read-write [R-W] circuits [7, 2006.01]
- 11/42 • • • using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically- or optically-coupled [1, 2006.01]
- 11/44 • • • using super-conductive elements, e.g. cryotron [1, 2, 2006.01]
- 11/46 • • • using thermoplastic elements [1, 2006.01]
- 11/48 • • • using displaceable coupling elements, e.g. ferromagnetic cores, to produce change between different states of mutual or self-inductance [1, 2006.01]
- 11/50 • • • using actuation of electric contacts to store the information (mechanical stores G11C 23/00; switches providing a selected number of consecutive operations of the contacts by a single manual actuation of the operating part H01H 41/00) [1, 2006.01]
- 11/52 • • • using electromagnetic relays [1, 2006.01]
- 11/54 • • • using elements simulating biological cells, e.g. neuron [1, 2006.01]
- 11/56 • • • using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency (counting arrangements comprising multi-stable elements of this type H03K 25/00, H03K 29/00) [2, 2006.01]
- 13/00 Digital stores characterised by the use of storage elements not covered by groups G11C 11/00, G11C 23/00, or G11C 25/00 [1, 2006.01]**
- 13/02 • • • using elements whose operation depends upon chemical change (using electrochemical charge G11C 11/00) [1, 2006.01]
- 13/04 • • • using optical elements [1, 2006.01]
- 13/06 • • • using magneto-optical elements (magneto-optics in general G02F) [2, 2006.01]
- 14/00 Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down [5, 2006.01]**
- 15/00 Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores (in which information is addressed to a specific location G11C 11/00) [1, 2, 2006.01]**
- 15/02 • • • using magnetic elements [2, 2006.01]
- 15/04 • • • using semiconductor elements [2, 2006.01]
- 15/06 • • • using cryogenic elements [2, 2006.01]
- 16/00 Erasable programmable read-only memories (G11C 14/00 takes precedence) [5, 2006.01]**
- 16/02 • • • electrically programmable [5, 2006.01]
- 16/04 • • • using variable threshold transistors, e.g. FAMOS [5, 2006.01]

- 16/06 • • Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00) [5, 2006.01]
- 16/08 • • • Address circuits; Decoders; Word-line control circuits [7, 2006.01]
- 16/10 • • • Programming or data input circuits [7, 2006.01]
- 16/12 • • • • Programming voltage switching circuits [7, 2006.01]
- 16/14 • • • • Circuits for erasing electrically, e.g. erase voltage switching circuits [7, 2006.01]
- 16/16 • • • • • for erasing blocks, e.g. arrays, words, groups [7, 2006.01]
- 16/18 • • • • Circuits for erasing optically [7, 2006.01]
- 16/20 • • • • Initialising; Data preset; Chip identification [7, 2006.01]
- 16/22 • • • Safety or protection circuits preventing unauthorised or accidental access to memory cells [7, 2006.01]
- 16/24 • • • Bit-line control circuits [7, 2006.01]
- 16/26 • • • Sensing or reading circuits; Data output circuits [7, 2006.01]
- 16/28 • • • • using differential sensing or reference cells, e.g. dummy cells [7, 2006.01]
- 16/30 • • • Power supply circuits [7, 2006.01]
- 16/32 • • • Timing circuits [7, 2006.01]
- 16/34 • • • Determination of programming status, e.g. threshold voltage, overprogramming or underprogramming, retention [7, 2006.01]

- 17/00 **Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards** (erasable programmable read-only memories G11C 16/00; coding, decoding or code conversion, in general H03M) [1, 2, 5, 2006.01]
- 17/02 • using magnetic or inductive elements (G11C 17/14 takes precedence) [2, 5, 2006.01]
- 17/04 • using capacitive elements (G11C 17/06, G11C 17/14 take precedence) [2, 5, 2006.01]
- 17/06 • using diode elements (G11C 17/14 takes precedence) [2, 5, 2006.01]
- 17/08 • using semiconductor devices, e.g. bipolar elements (G11C 17/06, G11C 17/14 take precedence) [5, 2006.01]
- 17/10 • • in which contents are determined during manufacturing by a predetermined arrangement of coupling elements, e.g. mask-programmable ROM [5, 2006.01]
- 17/12 • • • using field-effect devices [5, 2006.01]
- 17/14 • in which contents are determined by selectively establishing, breaking or modifying connecting links by permanently altering the state of coupling elements, e.g. PROM [5, 2006.01]
- 17/16 • • using electrically-fusible links [5, 2006.01]
- 17/18 • • Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00) [5, 2006.01]

- 19/00 **Digital stores in which the information is moved stepwise, e.g. shift registers** (counting chains H03K 23/00) [1, 2006.01]
- 19/02 • using magnetic elements (G11C 19/14 takes precedence) [2, 2006.01]
- 19/04 • • using cores with one aperture or magnetic loop [2, 2006.01]
- 19/06 • • using structures with a number of apertures or magnetic loops, e.g. transfluxors [2, 2006.01]
- 19/08 • • using thin films in plane structure [2, 2006.01]
- 19/10 • • using thin films on rods; with twistors [2, 2006.01]
- 19/12 • using non-linear reactive devices in resonant circuits [2, 2006.01]
- 19/14 • using magnetic elements in combination with active elements, e.g. discharge tubes, semiconductor elements (G11C 19/34 takes precedence) [2, 7, 2006.01]
- 19/18 • using capacitors as main elements of the stages [2, 2006.01]
- 19/20 • using discharge tubes (G11C 19/14 takes precedence) [2, 2006.01]
- 19/28 • using semiconductor elements (G11C 19/14, G11C 19/36 take precedence) [2, 7, 2006.01]
- 19/30 • using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically- or optically-coupled [2, 2006.01]
- 19/32 • using super-conductive elements [2, 2006.01]
- 19/34 • using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency [7, 2006.01]
- 19/36 • • using semiconductor elements [7, 2006.01]
- 19/38 • two-dimensional, e.g. horizontal and vertical shift registers [7, 2006.01]

- 21/00 **Digital stores in which the information circulates** (stepwise G11C 19/00) [1, 2006.01]
- 21/02 • using electromechanical delay lines, e.g. using a mercury tank [1, 2006.01]

- 23/00 **Digital stores characterised by movement of mechanical parts to effect storage, e.g. using balls; Storage elements therefor** (storing by actuating contacts G11C 11/48) [1, 2006.01]

- 25/00 **Digital stores characterised by the use of flowing media; Storage elements therefor** [1, 2006.01]

- 27/00 **Electric analogue stores, e.g. for storing instantaneous values** [1, 2006.01]
- 27/02 • Sample-and-hold arrangements (G11C 27/04 takes precedence; sampling electrical signals, in general H03K) [2, 4, 2006.01]
- 27/04 • Shift registers (charge coupled devices per se H01L 29/76) [4, 2006.01]

- 29/00 **Checking stores for correct operation; Testing stores during standby or offline operation** [1, 2006.01]
- 29/02 • Detection or location of defective auxiliary circuits, e.g. defective refresh counters [2006.01]
- 29/04 • Detection or location of defective memory elements [2006.01]
- 29/06 • • Acceleration testing [2006.01]
- 29/08 • • Functional testing, e.g. testing during refresh, power-on self testing [POST] or distributed testing [2006.01]
- 29/10 • • • Test algorithms, e.g. memory scan [MScan] algorithms; Test patterns, e.g. checkerboard patterns [2006.01]
- 29/12 • • • Built-in arrangements for testing, e.g. built-in self testing [BIST] [2006.01]
- 29/14 • • • • Implementation of control logic, e.g. test mode decoders [2006.01]
- 29/16 • • • • • using microprogrammed units, e.g. state machines [2006.01]
- 29/18 • • • • Address generation devices; Devices for accessing memories, e.g. details of addressing circuits [2006.01]
- 29/20 • • • • • using counters or linear-feedback shift registers [LFSR] [2006.01]

29/22	• • • • •	Accessing serial memories [2006.01]	29/46	• • • • •	Test trigger logic [2006.01]
29/24	• • • • •	Accessing extra cells, e.g. dummy cells or redundant cells [2006.01]	29/48	• • •	Arrangements in static stores specially adapted for testing by means external to the store, e.g. using direct memory access [DMA] or using auxiliary access paths (external testing equipment G11C 29/56) [2006.01]
29/26	• • • • •	Accessing multiple arrays (G11C 29/24 takes precedence) [2006.01]	29/50	• •	Marginal testing, e.g. race, voltage or current testing [2006.01]
29/28	• • • • •	Dependent multiple arrays, e.g. multi-bit arrays [2006.01]	29/52	•	Protection of memory contents; Detection of errors in memory contents [2006.01]
29/30	• • • • •	Accessing single arrays [2006.01]	29/54	•	Arrangements for designing test circuits, e.g. design for test [DFT] tools [2006.01]
29/32	• • • • •	Serial access; Scan testing [2006.01]	29/56	•	External testing equipment for static stores, e.g. automatic test equipment [ATE]; Interfaces therefor [2006.01]
29/34	• • • • •	Accessing multiple bits simultaneously [2006.01]	99/00	Subject matter not provided for in other groups of this subclass [2006.01]	
29/36	• • • • •	Data generation devices, e.g. data inverters [2006.01]			
29/38	• • • • •	Response verification devices [2006.01]			
29/40	• • • • •	using compression techniques [2006.01]			
29/42	• • • • •	using error correcting codes [ECC] or parity check [2006.01]			
29/44	• • • • •	Indication or identification of errors, e.g. for repair [2006.01]			