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(54) Title: DIGITAL HIGH-SPEED PRINTING SYSTEM ARCHITECTURE

(57) Abstract: A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). The video RAM devices (44) perform bi-directional image data block transfers between the dynamic band RAM (46) and the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port. A digital high-speed printing system architecture for processing contiguous raster-image data blocks for transmission to a marking engine, comprises a central processing unit ("CPU") (42) and at least one video RAM device (44). Each video RAM device (44) includes a dynamic band RAM (46), a serial access memory (48), a random access port for transmitting and receiving image data blocks to and from the dynamic band RAM (46), and a serial port for transmitting and receiving image data blocks to and from the serial access memory (48). Furthermore, the video RAM devices (44) transfer image data blocks to and from the serial access port, and simultaneously transfer of image data blocks to and from the random access port.

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